University Of Minnesota -Duluth

ECE 2212

Electronics I

Lab 10: BJT Current Sources

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Abstract

The purpose of this lab will be to extract some the parameters of internal resistance within a transistor. In class, we covered how to construct a Widlar current sink using a set of matched transistors. In class, we covered what "matched" means regarding the width and length along with series of other significant parameters. In the lab, by using transistors from the same batch the thermal exposure as well as the fact they're 'matched' will work as a way of fixing the transistors to equally distribute the load between the two which is effectively how the Widlar works. If the transistor(s) is unmatched, this will lead to skew or veering of current to one side over another.

Introduction

This lab will cover the implementation of the Widlar current source and sink using matched transistors from a single array. We will measure the IV characteristics of this to extract the output resistance using linear regression.

Background

For additional references see chapter 3 of Microelectronics Circuit Design 5^{th} Ed or the ECE 2212 course page.

Procedure

Using the Schematic in Fig 1 as a reference connect collector of Q2 to the variable 12-Volt DC supply. Using either the DMM or the Oscope measure the voltage V_R across R_1 with the realization that $I_{C2} = \frac{V_R}{1K}$. Then adjust the potentiometer to set $I_{C2} = 1mA$. Comparing the values with the reference current. Using the data obtained construct an I-V output characteristic curve by dialing V_{C2} from 0 to 6 volts. Using LtSpice model the circuit construction and modify V_{AF} and β_F accordingly. Take the tabular data and recording it in google sheets to find the linear regression of it. Find the slope of the linear fit and use this to get R_{out}. For the plot on the

Materials needed for lab:

- LM3046/CA3046 Transistor array
- 12± Volt Power Supply 6
- 0.01mF capacitor
- 2× 2N2222 NPN transistors
- $26.8\,\mathrm{K}\Omega, 4.7\,\mathrm{K}\Omega$

0.1 Equations

An equivalent model will be derived using the *Shichman and Hodges level-1 model* equations for BJT transistor.

$$V_T = \frac{kT}{q} \tag{1}$$

$$I_{REF} = \frac{\beta}{\beta + 1} * I_E \tag{2}$$

$$R_2 = \frac{V_T}{(1 + \frac{1}{\beta_2})I_C} * ln(\frac{I_{C1}}{I_{C2}}) \tag{3}$$

Use the `.Step Param R start end increment` where `R` the symbolic variable for the value to simulate variable resistance with Ltspice directives

0.2 Schematics

The Circuit schema for both the simulation and layout on breadboard. Schema for lab 8 is on the left while the schema for lab 9 is on the right. For our particular widlar circuit we used pins 5-11 on the array.

Table 1: **Widlar Current Mirror Setup in LtSpice**

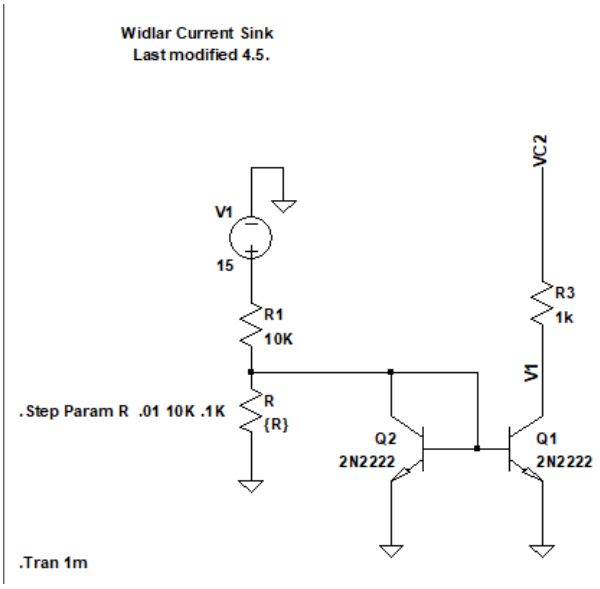
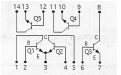


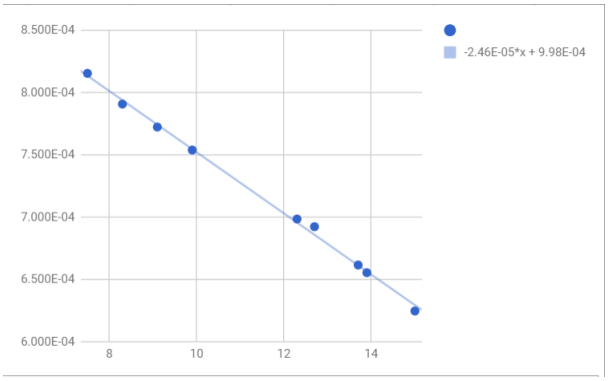
Table 2: Pinout For the CA3046 Transistor array

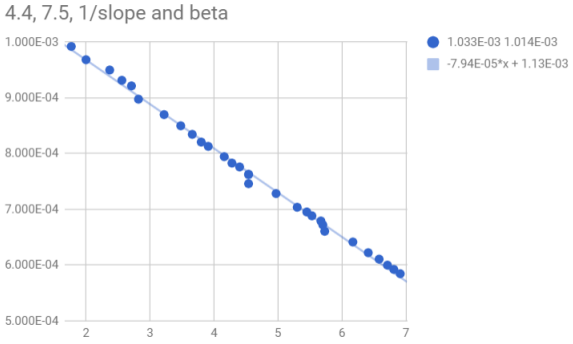


Measurement and Analysis of Results:

In this experiment, we performed two separate forms of analysis on the same concept to verify that the same was true for the array. We calculate the $R_{out} = \frac{1}{slope}$ of the linear regression. From the datasheet, you can see that the R_{out} resistance was the same and that we obtained a high correlation for two distinctly separate models. For the plot on the left we found $R_{out} = 40.65\,\text{K}\Omega$ and for the model on the right the one the was constructed from the transistor array we found $R_{out} = 12.59\,\text{K}\Omega$

Table 3: Semilog Plot of V_2 vs I_C





Conclusion

Though we were able to get the results we wanted. The lab results were consistent with what you would expect from the datasheet and consistent with itself. We found a high correlation with the data on the graph with the model. An interesting idea for a lab would be to construct and observe the properties of the BJTs with a widlar circuit whlist driving an increasing load. Furthermore it would be interesting to use 3 transistors instead of 2 in a 'tricycle' configuration to see if it lends itself to a more stable current source.